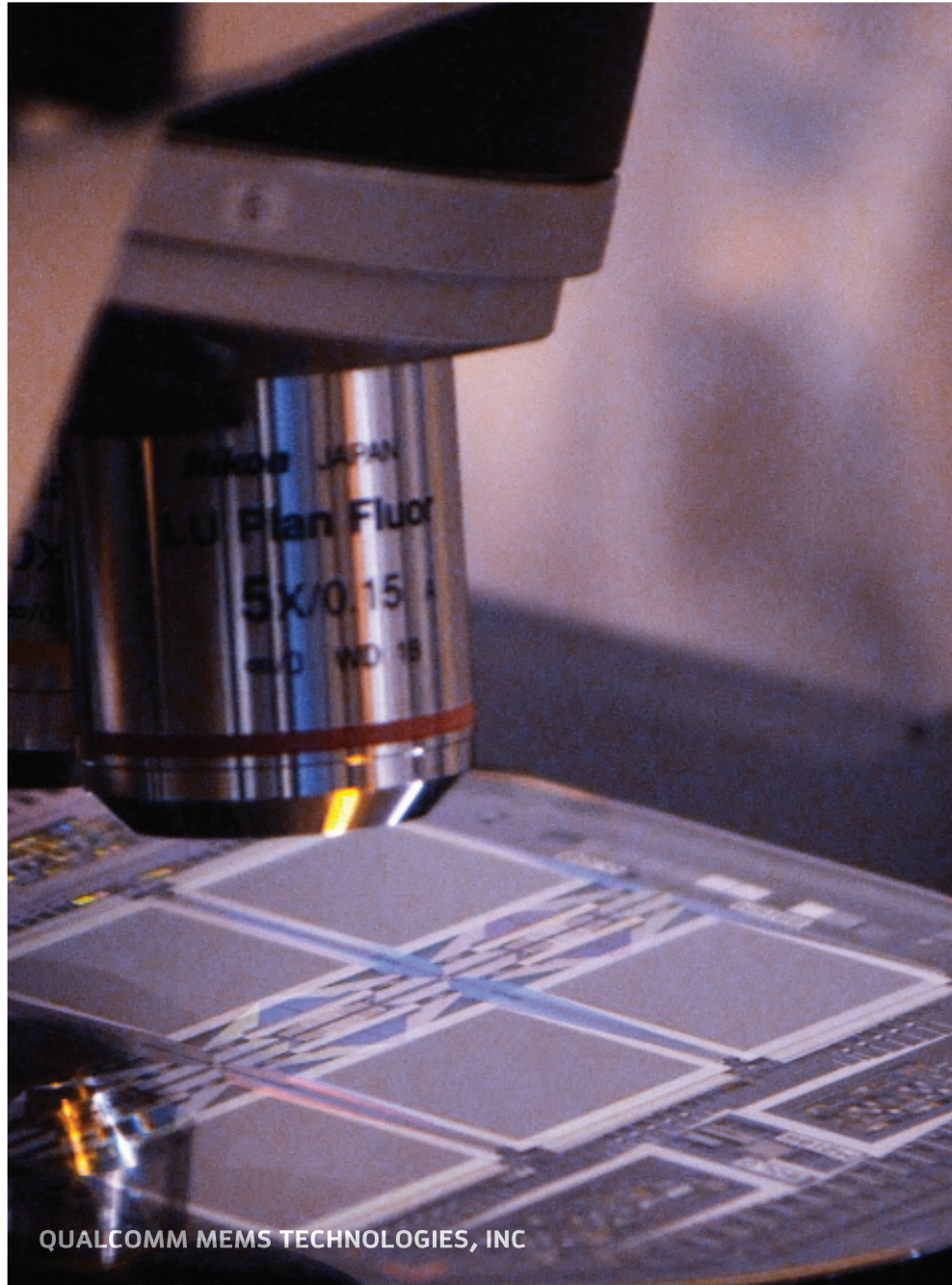


# Operating Principles of the IMOD Drive



QUALCOMM MEMS TECHNOLOGIES, INC



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### Executive Summary

Interferometric Modulator (IMOD) technology is the revolutionary technology found in Qualcomm's mirasol® displays. Based upon micro-electro-mechanical systems (MEMS), IMOD technology in mirasol displays enables reflective, direct view, flat panel displays. The structure exploits interference, providing a highly efficient reflective display which enables superior viewability across a wide range of ambient viewing conditions. The electro-mechanical behavior of the MEMS device provides bistability, in turn providing low power consumption. IMOD pixels are capable of switching speeds on the order of microseconds, enabling video-rate-capable displays. mirasol displays, fabricated using IMOD technology, have demonstrated reflectivities of greater than 60 percent, contrast ratios greater than 15:1 and drive voltages below 5 volts. Though simple in structure, mirasol display's IMOD elements provide the functions of light modulation, color selection and memory while replacing the functionality provided by polarizers, liquid crystal, color filters, and active matrices found in Liquid Crystal Displays (LCD).

This paper outlines the basic operating principles of a mirasol display and how its electro-mechanical and electro-optical characteristics allow the panel to be addressed with a passive matrix drive scheme. Operational similarities and differences to existing passive-matrix liquid-crystal displays will also be highlighted.

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### Structure and Electro-Mechanical Properties of an IMOD Pixel in a mirasol Display

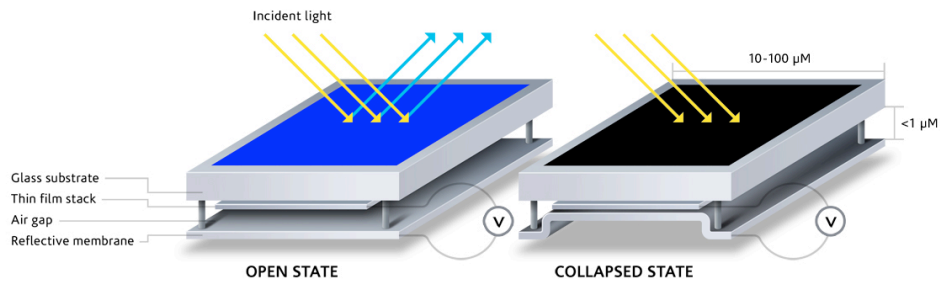


Figure 1. Basic Structure of an IMOD Pixel

Figure 1 illustrates the basic structure of an IMOD element; a mirasol display pixel is comprised of any number of these elements. These elements are fabricated on a glass substrate using standard thin-film processes, creating an optically resonant MEMS cavity that comprises an air gap separating a stack of optical thin films from a movable reflective membrane. The optical gap between a partial reflector (within the thin film stack) and the reflective membrane is chosen such that light reflecting within this optical gap exhibits constructive and destructive interference. The wavelength at which constructive interference occurs sets the color of the light reflected by the IMOD element. Altering the height of the air gap portion of the cavity leads to the reflection of different colors of light.

The application of a voltage between the membrane and thin-film stack creates an electrostatic field. When the field exceeds a given threshold, the electrostatic field causes the membrane to collapse as shown in Figure 1. This state is called the collapsed state and the element appears black since there is destructive interference across the visible spectrum. Reducing the applied voltage below an additional threshold releases the membrane, which travels back to the original position called the open state. In this position the IMOD element is bright and tuned to reflect a particular color. The difference in threshold voltages for actuation and release creates a condition known as hysteresis that together with the non-linear electro-optical response is exploitable for matrix addressing.

### Memory in an IMOD element

Memory in an IMOD element is enabled by a linear mechanical force competing with a nonlinear electrostatic force. This difference creates hysteresis in the IMOD element and provides it with bistable behavior. This in turn can be exploited as pixel memory. The basic IMOD electro-mechanical structure can be idealized as shown in Figure 2. The structure consists of a fixed electrode (i.e., the thin-film stack), above which the flexible reflective membrane is suspended. The flexible reflective membrane can be envisioned as a simple linear spring (of spring constant  $k$ ) from which a mirror of surface area  $A$  is suspended. With no potential difference applied to the system, the mirror is at rest a distance  $d$  from the fixed electrode.

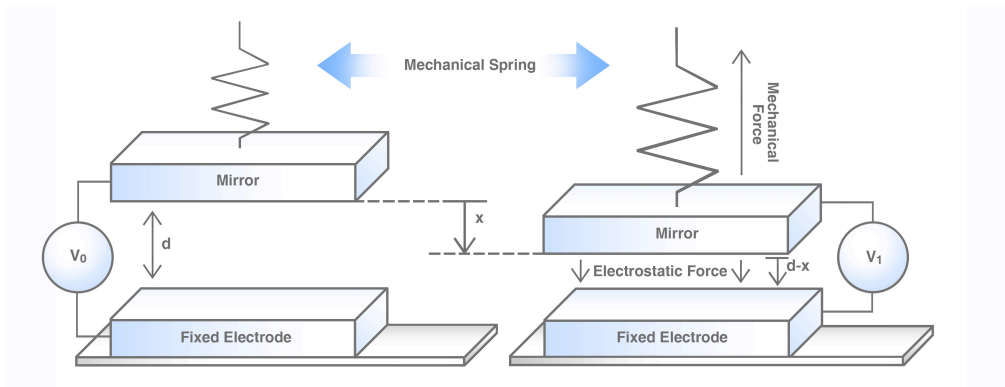


Figure 2. IMOD Pixel Represented as a Mirror Suspended on a Mechanical Spring

On the application of a potential difference  $V_1$  between the fixed electrode and mirror, electrostatic attraction occurs. Equilibrium in this system results when the mechanical force applied by the spring equals this attractive electrostatic force, which occurs after the mirror has undergone a displacement  $x$ , and comes to rest at a distance  $d-x$  away from the fixed electrode.

The mechanical force can be defined as:

$$F_{Spring} = -kx \quad (1.1)$$

The electrostatic force can be defined as:

$$F_{Electrostatic} = \frac{1}{2} \frac{\epsilon A}{(d-x)^2} V^2 \quad (1.2)$$

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At equilibrium the net force must be zero. Therefore:

$$F = \frac{1}{2} \frac{\epsilon A}{(d-x)^2} V^2 - kx = 0$$

Or

$$kx = \frac{1}{2} \frac{\epsilon A}{(d-x)^2} V^2 \tag{1.3}$$

Plotting the two forces as a function of membrane position, as shown in Figure 3, shows the relationship between the membrane position and the voltage applied to the IMOD element. The dotted black line represents the linear mechanical force  $F_{\text{Spring}}$ , while the curved colored lines represent the nonlinear electrostatic force  $F_{\text{Electrostatic}}$  at varying voltage levels.

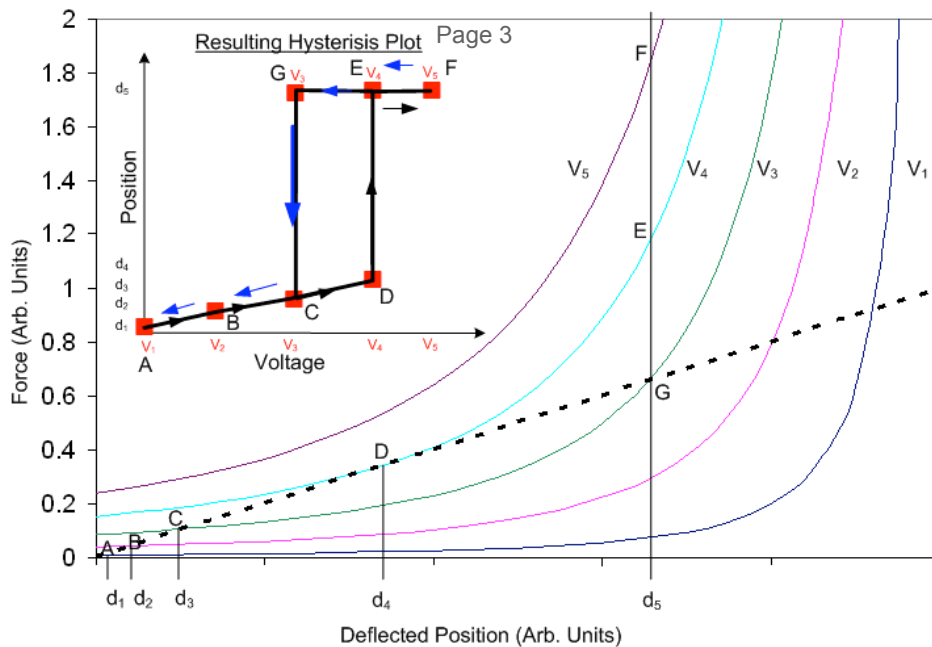


Figure 3. Linear Restoring Force vs. Nonlinear Attractive Force Results in Hysteresis

As the voltage applied to the system is increased from  $V_1$  through  $V_4$ , the membrane position moves a distance  $d_1$  to  $d_4$ , the distances signifying the membrane positions where the two competing forces are equal. At any voltage greater than  $V_4$  (labeled point D in the figure), the electrostatic force is greater than the mechanical force. This is a critical point beyond which the mechanical force can not counterbalance the electrostatic force and the membrane continues to deflect until it contacts the thin film stack, at a distance labeled  $d_5$ . Further application of voltage increases the

electrostatic field between the membrane and bottom electrode, but no further deflection or change in optical response occurs since the membrane is already in contact with the thin film stack.

As the applied voltage is reduced from  $V_5$ , the electrostatic force remains greater than the mechanical force until the voltage  $V_3$  is reached, at which point the curves depicting the electrostatic and mechanical forces intersect at the deflection  $d_5$  denoted in the figure as point G. A further decrease in voltage below  $V_3$  makes the mechanical force greater than the electrostatic force, causing the membrane to snap back to the open state and deflection  $d_3$  (point C in the figure). Plotting the membrane position as a function of voltage, as shown in the inset plot in Figure 3, shows the resulting hysteresis. The black arrows show the membrane position as a function of increasing voltage, while the blue arrows indicate decreasing voltage. The membrane releases from the collapsed state to the open state at a lower voltage than the actuation voltage required to move the pixel from the open state to the collapsed state.

This hysteresis creates the bistable behavior in the IMOD which allows a mirasol display to be addressed in a passive matrix form.

### Exploiting Hysteresis

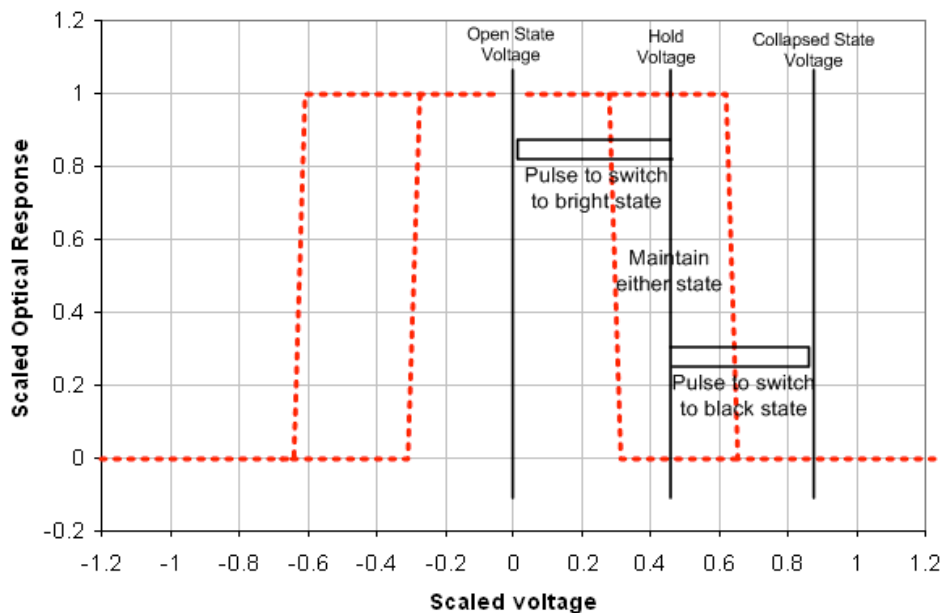


Figure 4: An IMOD Element's Hysteretic Electro-Optical Response Illustrating the Three Voltages Required to Drive the System.

Figure 4 illustrates the electro-optical behavior of a mirasol display. The three minimum voltage levels required to operate the device are also depicted in the



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figure—the Collapsed State, Hold and Open State voltages. By continuously applying a hold voltage across the IMOD element, a short activation voltage pulse is enough to cause the membrane to snap into the collapsed state and maintain that position upon the return to the hold voltage. Similarly, applying a short release voltage pulse causes the membrane to snap to the open state and to remain so upon the return to the hold voltage. This bistability can be exploited as described later. In contrast to an LCD, which must be continuously refreshed in order to prevent the displayed image from fading, the mirasol display requires no refreshing unless the frame data changes.

### IMOD Addressing

Addressing is the mechanism by which pixels are turned on and off. There are essentially two types of addressing schemes, direct and multiplexed. *Direct addressing* requires a dedicated control line/driver for every pixel. This scheme is used in some segmented displays such as the seven segment LCDs found in wrist watches and other low-pixel-density displays. *Multiplexed addressing* can drive a larger number of ordered pixels via their row and column address, significantly reducing the complexity of the circuit because each pixel no longer needs a dedicated circuit. For example, in a 10x10 matrix of pixels, direct addressing requires 100 drivers; multiplexing requires only 20, one for each row and column.

Flat-panel displays typically consist of an array of pixels, arranged in a rectangular matrix. The pixels are located at the intersection of the row and column electrodes, the electrodes themselves being patterned on the two substrates which make up the display. Typically, the electrodes are constructed of a semitransparent conductive material. In a passive-matrix liquid-crystal display, the two aforementioned substrates constrain the liquid crystal such that applying a voltage to electrodes of particular rows and columns creates an electric field across the LC material at the intersection of these electrodes. In the case of a mirasol display, as shown in Figure 1, the rows are conductive traces patterned within the thin-film stack, while the reflective membranes are tied together to form columns. In both cases, the pixel can be thought of as a small capacitor connecting the row and column electrodes, as shown in Figure 5, with the column drivers connected to the reflective conductive membranes and the row drivers connected to the patterned conductive electrodes.

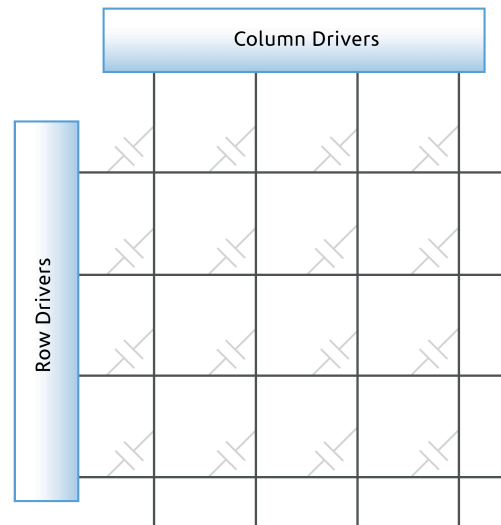


Figure 5. Passive Matrix LCD/mirasol Schematic

In the case of an LCD, due to the nonlinear electro-optical response curve, the passive pixel is addressed when the electric field across it passes a certain threshold and causes the LC molecules to align parallel to the field. When addressed via the row and column electrodes, the pixels have a short “turn on” time during which the LC molecules align themselves to the field. When the voltage is removed, the pixel behaves similar to a discharging capacitor and slowly “turns off,” allowing the LC molecules to return to their original orientation. Due to response times which are on the order of a few to few hundred milliseconds, the root mean square (RMS) voltage of the applied electric field characterizes the response of the LCD rather than the instantaneous voltage across a pixel. A display can scan across the matrix of pixels one row at a time, turning on and off the appropriate pixels. As long as the time to scan across all rows is shorter than the turn-off time, an image can be displayed. However, due to the RMS response of the LC, the display must be continuously refreshed to prevent the displayed image from degrading, even if the frame data does not change.

In the case of a mirasol display, each row in the display must be electrically driven until the IMOD element has responded, which is on the order of microseconds, before moving on to the next row. Once the pixel has been addressed by a short pulse to switch it to the collapsed or open state, and as long as the voltage across the pixel returns to the hold voltage after the pulse, the image will persist and no refresh is required to maintain it.

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In an LCD, the row and column voltages must be inverted after addressing all rows in order to prevent a DC field across the pixel, as this field tends to cause ion migration in the LC material.

The mirasol display drive schemes make use of both polarities of the hysteresis curve in order to maintain neutrality in the thin film stack, as explained below.

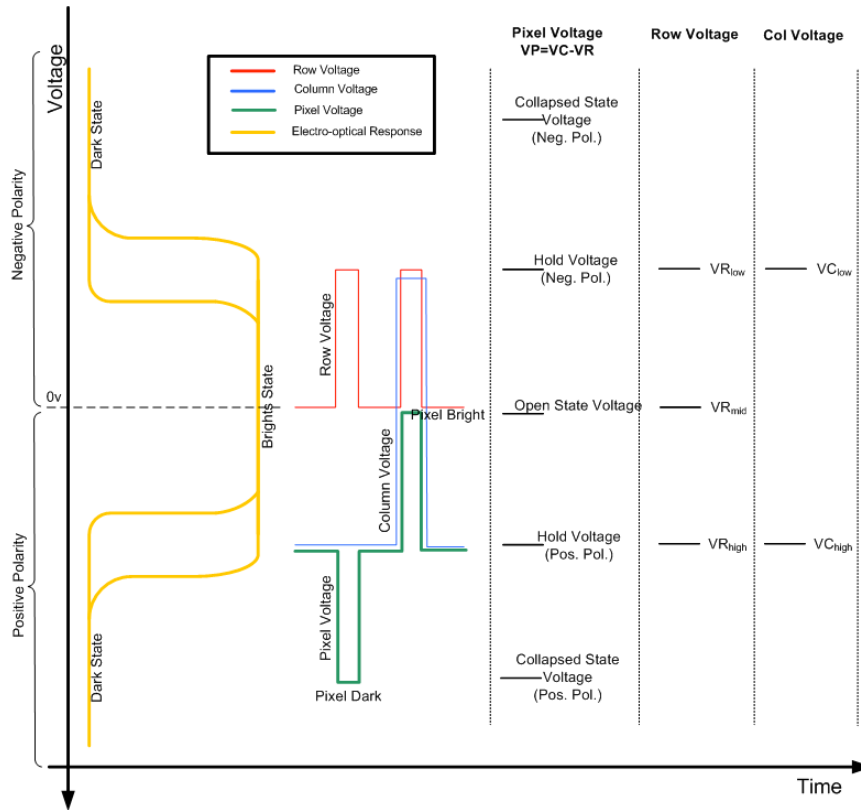


Figure 6. IMOD Hysteresis Curve and Associated Row and Column Waveforms Required for Switching a Pixel “On” and “Off.”

	$VC_{low}$	$VC_{high}$
$VR_{low}$	Pixel Value: Release Pixel Polarity: +	Pixel Value: Activate Pixel Polarity: +
$VR_{mid}$	Pixel Value: Hold Pixel Polarity: -	Pixel Value: Hold Pixel Polarity: +
$VR_{high}$	Pixel Value: Activate Pixel Polarity: -	Pixel Value: Release Pixel Polarity: -

Table 1: Complete Set of Pixel Voltages Based on the Three Possible Row and Two Possible Column Voltages

Figure 6 illustrates the electro-optical curve shown in Figure 4, rotated 90°. Placing this curve along with the row (VR) and column (VC) waveforms on the time axis shows how the pixel voltage ( $VP=VC-VR$ ) can be switched to provide a collapsed and open state, i.e. “dark pixel” and “bright pixel.” Table 1 defines the complete set of pixel voltages and associated IMOD pixel states. Note that the appropriate selection of VR and VC voltages allows use of both polarities of the electro-optical curve.

As shown in Figure 6, the waveforms start with the row voltage VR at 0V ( $VR_{mid}$ ) and VC at  $VC_{high}$  resulting in the pixel voltage being set to the hold voltage in the positive polarity. At the start of the row pulse, VR swings to  $VR_{low}$  which causes the voltage across the pixel to pulse high (collapsed state voltage) and the pixel is turned dark. At the end of the pulse VR returns to  $VR_{mid}$ , the pixel voltage returns to the hold voltage level and the pixel stays dark.

In order to turn the pixel to the bright state, a release pulse must be applied. For this to occur, VR is once again swung to  $VR_{low}$ , but this time VC swings to  $VC_{low}$ , the resulting voltage on the pixel is 0V and the pixel is released to the bright state. As VR returns to  $VR_{mid}$  and VC returns to  $VC_{high}$  the pixel is held in the open state.

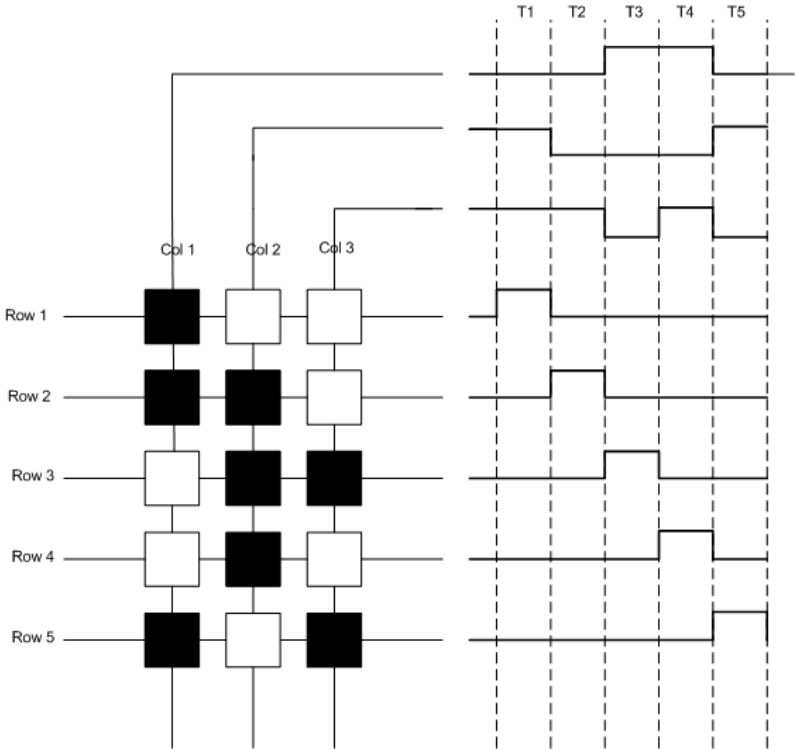


Figure 7: Example Row and Column Waveforms for Addressing an Array of 15 IMOD Pixels

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Figure 7 illustrates the addressing of a 15-pixel display along with the drive waveforms for the row and columns which set the pixels into their depicted state. At time T1, row 1 is pulsed high to  $VR_{high}$ . When row 1 pulses, it latches the column data for column 1 ( $VC_{low}$ ), column 2 ( $VC_{high}$ ), and column 3 ( $VC_{high}$ ). The resultant potential difference across the pixels places the membranes in Row 1 into the dark state for the first pixel and bright state for the last two pixels. At time T2, Row 1 settles to  $VR_{mid}$  and the pixels maintain their state as they are now in the hold state since  $VC_{high} - VR_{mid} = \text{hold voltage}$ . Simultaneously, Row 2 pulses high and latches the column data for Columns 1 thru 3. Since the column waveforms for Columns 1 and 3 are unchanged ( $VC_{low}$ ) from time T1, only column 2 changes state from  $VC_{high}$  to  $VC_{low}$ .

At time T3, Row 2 settles to  $VR_{mid}$  and the pixels are now in the hold state. The remaining values for Rows 3 through 5 are determined one row at a time as explained above. By appropriate selection of  $VR_{high}$  or  $VR_{low}$  the data to the display can be written and held in either the negative or positive polarity. Once all rows have been addressed, the display is in the hold state by maintaining column data and placing all rows at  $VR_{mid}$ . In this state the data is maintained on the display and no further action is required until new frame data is written to the display.

The addressing time required for the column voltages to reach their final state must be less than the pixel response time, which in turn should be less than or equal to the line time. Therefore: Pixel Voltage Settling Time < Pixel Response Time  $\leq$  Line Time. Since the pixel response time is on the order of microseconds, a complete row of data in a mirasol display can be written in roughly the same time.

Figure 8 illustrates a sample “Rip and Hold” drive scheme which takes advantage of the bistable nature of the mirasol display. During the “Rip” period (which is always less than the frame time), every row of the mirasol display is updated, after which the display is placed in the “Hold” state. Once the frame data is changed, another display update session is triggered during which all the rows get sequentially addressed and placed in the hold state. Note that the rip and frame times are independent of each other; as shown in Figure 8, the rip rate is based on system requirements. The frame time is determined by the application driving the display. The application may choose to update the display as early as the end of the rip period or only as needed, maximizing power savings.

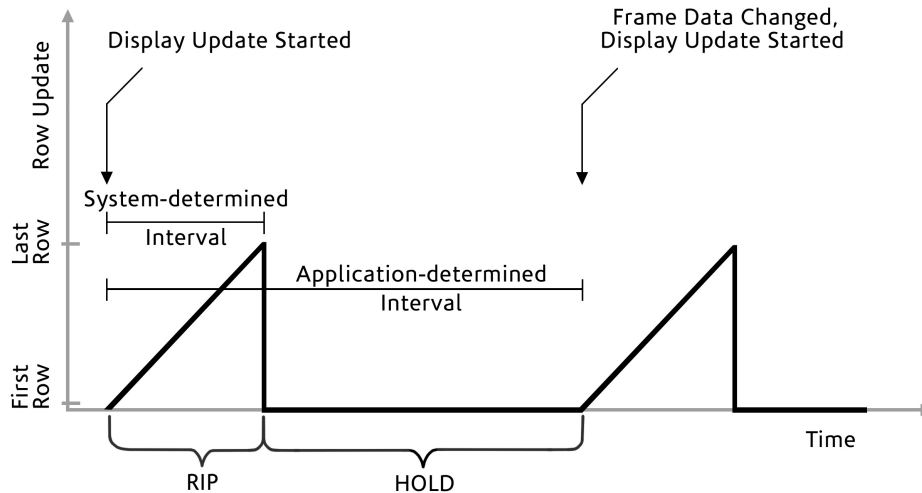


Figure 8: Rip and Hold Drive Scheme Functionality in a mirasol Display

## Conclusion

The mirasol display's IMOD element's electro-mechanical response provides three key benefits, all based on its inherent hysteresis behavior:

1. The hysteresis loop provides for a voltage regime where both on and off states are stable (bistability), providing memory and power savings.
2. The hysteretic nature of the IMOD element provides the fundamental nonlinear optical response that enables multiplexing.
3. The rapid response of the small IMOD structure allows the pixel to rapidly transition the hysteresis loop, leading to fast frame updates and video-capable displays.

For more information about mirasol display technology, visit

[www.mirasoldisplays.com](http://www.mirasoldisplays.com)

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